PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently amended) ~~A communication device~~ An apparatus, comprising:

a mapper ~~for~~ receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller ~~for~~ directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

2. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the first and second values are In-phase (I) and Quadrature (Q) values, respectively.

3. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the third values are soft decision values.

4. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the third values are Log Likelihood Ratio (LLR) values.

5. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the plurality of memory banks comprise a number equal to twice the number of the plurality of third values.

6. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein two or more stored third values may be retrieved from two or more of the plurality of memory banks simultaneously.

7. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the controller directs the plurality of third values for storage in the plurality of memory banks using a storage pattern selectable from a plurality of storage patterns, the storage pattern selected in accordance with one of a plurality of transmission formats.

8. (Currently amended) The apparatus ~~communication device~~ of claim 7, wherein the plurality of transmission formats comprises 16 Quadrature Amplitude Modulation (QAM).

9. (Currently amended) The apparatus ~~communication device~~ of claim 7, wherein the plurality of transmission formats comprises 8 Phase Shift Keying (PSK).

10. (Currently amended) The apparatus ~~communication device~~ of claim 7, wherein the plurality of transmission formats comprises Quadrature Phase Shift Keying (QPSK).

11. (Currently amended) The apparatus ~~communication device~~ of claim 7, wherein the plurality of transmission formats comprises rate 1/3 encoding.

12. (Currently amended) The apparatus ~~communication device~~ of claim 7, wherein the plurality of transmission formats comprises rate 1/5 encoding.

13. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the plurality of memory banks are sized in accordance with one or more encoder packet sizes.

14. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of

the memory banks in the selected subset for storing one of the plurality of third values, respectively.

15. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the bank selection, offset selection, and third value selection are assigned in accordance with an encoding sequencing pattern.

16. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the number of cycles is six, and wherein:

the first cycle indicates first, third, fifth, and seventh memory banks are selected, with an offset of zero;

the second cycle indicates first, second, fifth, and sixth memory banks are selected, with respective offsets of one, zero, one, and zero;

the third cycle indicates second, third, seventh, and eighth memory banks are selected, with respective offsets of one, zero, one, and zero;

the fourth cycle indicates second, fourth, sixth, and eighth memory banks are selected, with an offset of one;

the fifth cycle indicates first, second, fifth, and sixth memory banks are selected, with an offset of two; and

the sixth cycle indicates second, third, seventh, and eighth memory banks are selected, with an offset of two.

17. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the number of cycles is six, and wherein:

the first cycle indicates first, third, and fifth memory banks are selected, with an offset of zero;

the second cycle indicates second, third, and sixth memory banks are selected, with respective offsets of zero, one, and zero;

the third cycle indicates first, fourth, and fifth memory banks are selected, with respective offsets of one, zero, and one;

the fourth cycle indicates second, fourth, and sixth eighth memory banks are selected, with an offset of one;

the fifth cycle indicates first, fourth, and fifth memory banks are selected, with an offset of two; and

the sixth cycle indicates second, third, and sixth memory banks are selected, with an offset of two.

18. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the number of cycles is six, and wherein:

the first cycle indicates first and third memory banks are selected, with an offset of zero;

the second cycle indicates second and first memory banks are selected, with respective offsets of zero and one;

the third cycle indicates fourth and third memory banks are selected, with respective offsets of zero and one;

the fourth cycle indicates second and fourth memory banks are selected, with an offset of one;

the fifth cycle indicates first and second memory banks are selected, with an offset of two; and

the sixth cycle indicates third and fourth memory banks are selected, with an offset of two.

19. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the number of cycles is ten, and wherein:

the first cycle indicates first and third memory banks are selected, with an offset of zero;

the second cycle indicates second and first memory banks are selected, with respective offsets of zero and one;

the third cycle indicates fourth and third memory banks are selected, with respective offsets of zero and one;

the fourth cycle indicates second and first memory banks are selected, with respective offsets of one and two;

the fifth cycle indicates fourth and third memory banks are selected, with respective offsets of one and two;

the sixth cycle indicates second and fourth memory banks are selected, with an offset of two;

the seventh cycle indicates first and third memory banks are selected, with an offset of three;

the eighth cycle indicates second and first memory banks are selected, with respective offsets of three and four;

the ninth cycle indicates fourth and third memory banks are selected, with respective offsets of three and four; and

the tenth cycle indicates second and fourth memory banks are selected, with an offset of four.

20. (Currently amended) The apparatus ~~communication device~~ of claim 14, wherein the number of cycles in a storage pattern is twice the number of encoded symbols in an associated encoding sequence pattern.

21. (Currently amended) The apparatus ~~communication device~~ of claim 1, further comprising a plurality of muxes for receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by the controller.

22. (Currently amended) The apparatus ~~communication device~~ of claim 1, further comprising a plurality of tri-state buses for connected to the plurality of memory banks, each tri-state bus for receiving a third value, selectable by the controller, and each memory bank operable to store the value of the respective tri-state bus as directed by the controller.

23. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the controller produces a storing address for one or more memory banks according to the storing pattern, each storing address computed using a base address added to an offset indicated by the

storing pattern, the base address incremented by a fixed amount subsequent to completion of each successive iteration of the storing pattern.

24. (Currently amended) The apparatus ~~communication device~~ of claim 23~~1~~, wherein the base value is set to an initial value and reset to the initial value once a predetermined number of third values have been stored.

25. (Currently amended) The apparatus ~~communication device~~ of claim 1, wherein the controller selects two or more memory banks for simultaneous retrieval of stored third values according to an address, the address being incremented sequentially subsequent to each simultaneous retrieval.

26. (Currently amended) The apparatus ~~communication device~~ of claim 1, further comprising a decoder for receiving a series of two or more fourth values and decoding a plurality of fifth values therefrom.

27. (Currently amended) The apparatus ~~communication device~~ of claim 26, wherein the decoder is a turbo decoder.

28. (Currently amended) The apparatus ~~communication device~~ of claim 1, further comprising a demodulator for demodulating a received signal to produce the first and second values.

29. (Currently amended) A wireless communication system including a ~~communication device~~ deinterleaver, comprising:

a mapper ~~for~~ receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller ~~for~~ directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

30. (Currently amended) A method for deinterleaving, comprising:

receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value,

mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values; and

simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

31. (original) The method of claim 30, further comprising:

producing a storing address for one or more memory banks according to the storing pattern, each storing address computed using a base address added to an offset indicated by the storing pattern; and

incrementing the base address by a fixed amount subsequent to completion of each successive iteration of the storing pattern.

32. (original) The method of claim 30, wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively.

33. (original) The method of claim 30, further comprising:

simultaneously retrieving two or more stored third values from two or more memory banks according to a retrieval address; and

incrementing the retrieval address sequentially subsequent to a simultaneous retrieval.

34. (original) The method of claim 33, further comprising delivering the retrieved stored third values to a decoder for subsequent decoding therefrom.

35. (Currently amended) A device, comprising:

means for receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value,

means for mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values; and

means for simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

36. (Currently amended) Computer readable media operable to perform the following steps:

receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value,

mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values; and

simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.